Supplementary materials for "Large-scale optical programmable logic array for two-dimensional cellular automaton"

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S1: Experimental setup of the optical programmable logic array

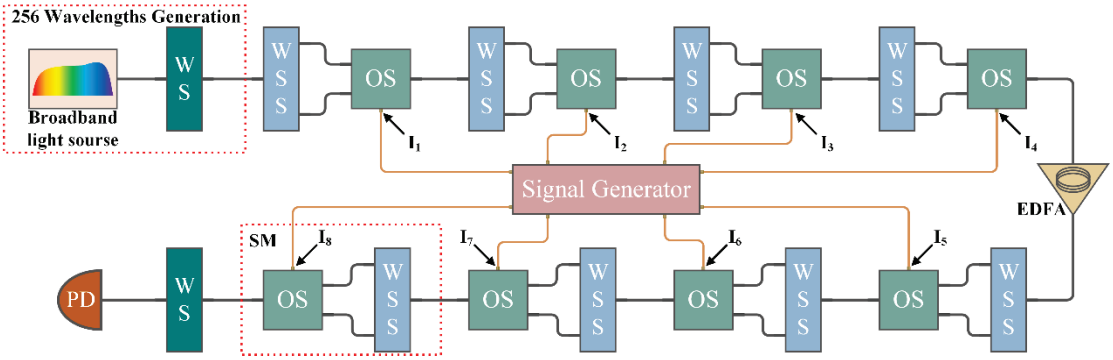

Fig. S1. Experimental setup of the eight-input programmable logic array (PLA) based on parallel spectrum modulation.WS, waveshaper; WSS, wavelength selective switch; OS, optical switch; SM, spectral modulators; EDFA, erbium doped fiber amplifier; PD, photodetector.

Fig. S1 shows the experimental implementation of the eight-input PLA. We use a broadband light source and a WS to generate 256 beams with an interval of 0.15 nm. The 256 beams are then modulated by eight cascaded SMs consisting of a WSS and a 1×2 OS. Considering the power loss caused by the optical components, an EDFA is added between the fourth and fifth SMs. After the last SM, a WS is used to select the target wavelength channels. The final logic computation results are detected by a PD.

To validate the high-speed computing capacity of the proposed PLA, we load high-speed signals at 10 Gbit/s to the OSs in the first and fifth SMs (Signals A_1 and B_1 of the four-bit comparator). Owing to the jitter of the single wavelength generated by the broadband light source, the beams corresponding to the logic minterms of the targeted logic functions are replaced by the outputs of the lasers.

S2: Demonstration of the four-bit adder and multiplier by PLA

Figs. S2 and S3 show the power distributions of the four-bit adder and multiplier, respectively. The extinction ratio between high and low levels exceeds 9 dB. The contrast between these two levels determines the accuracy of the final computation results.

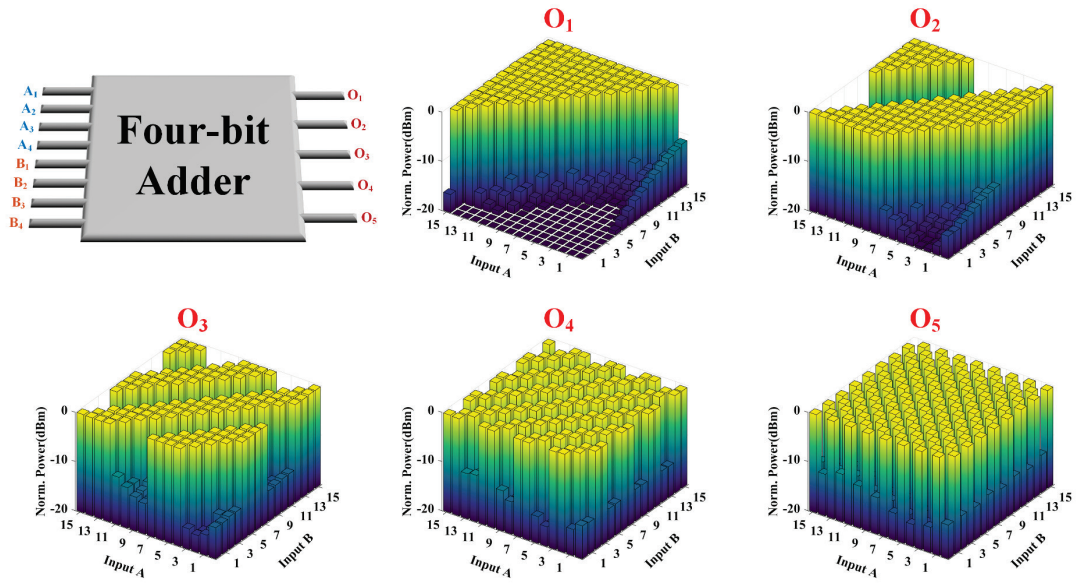

Fig. S2. Power distributions of the four-bit adder with five output ports ($O_1O_2O_3O_4O_5$).

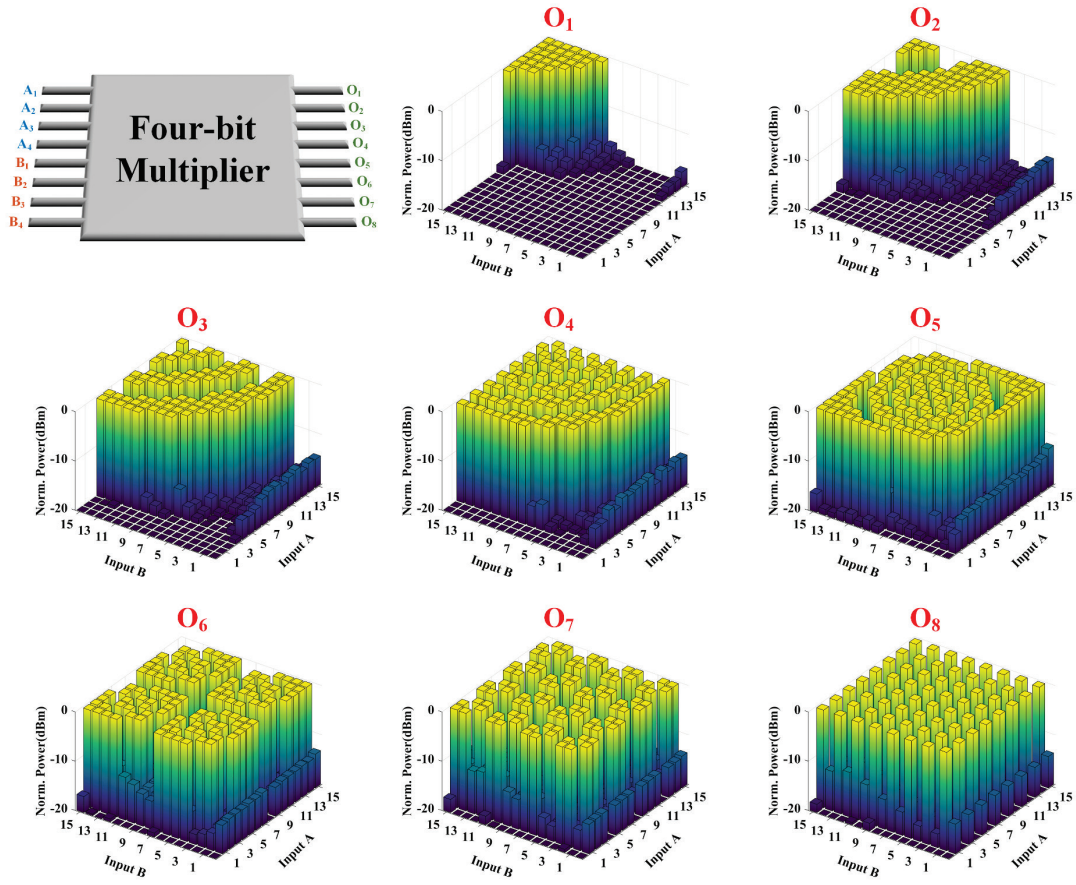

Fig. S3. Power distribution of the four-bit multiplier with eight output ports (O_1…O_8).

Fig. S4 shows the digital computing results of the 4-bit adder and multiplier. The input Signal A ($A_1A_2A_3A_4$) varies like a triangular waveform and Signal B ($B_1B_2B_3B_4$) varies like a gradual step-up waveform. The binary computing results are derived from output ports of the 4-bit adder and multiplier and converted into the decimal format shown in Fig. 4(c). As long as each output port performs the targeted logic operations, the final results will be accurate, which is ensured by the satisfactory extinction

ratio.

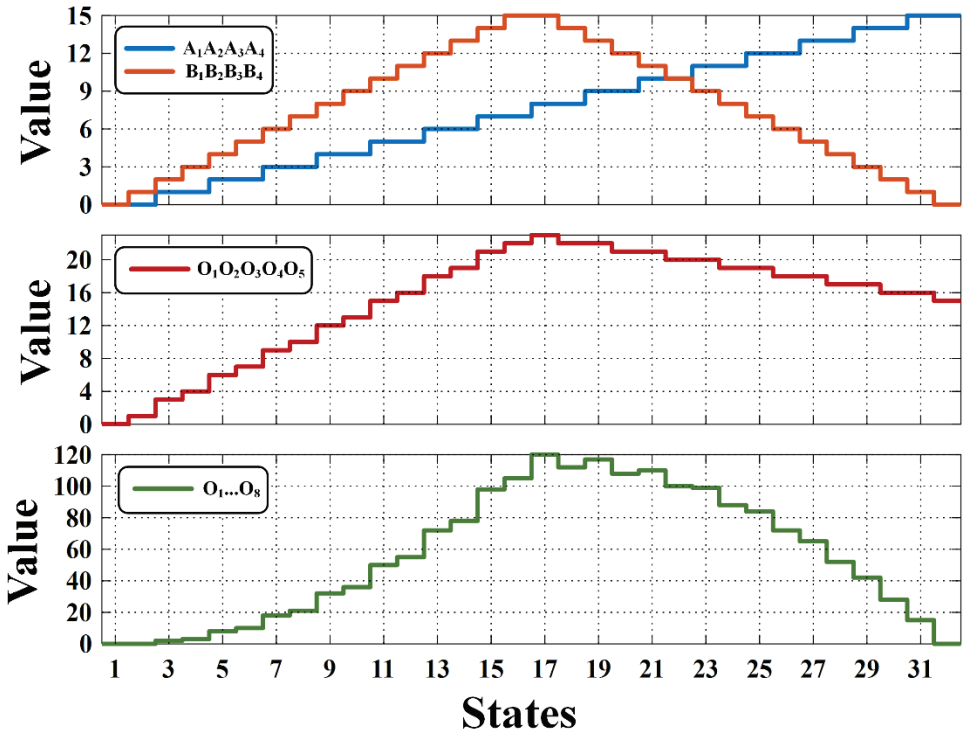

Fig. S4. The decimal values of Signal A ($A_1A_2A_3A_4$) and Signal B ($B_1B_2B_3B_4$), output results of the 4-bit adder ($O_1O_2O_3O_4O_5$) and 4-bit multiplier ($O_1 \ldots O_8$) in decimal form.

S3: The power distributions of statement machines

Based on 9-input PLA, we demonstrate two different state machines shown in Figs. 3(b) and 3(c). Fig. S5 illustrates the power distributions of the state machine to infer the date (month and day) according to the provided day of the year in all scenarios. We encode the day of the year (1-365) into a 9-bit binary number ($I_1 \ldots I_9$). To achieve a higher extinction ratio, the output states corresponding to the binary number outside the range of 1-365 are set to Logic 0. Fig. S6 shows the power distributions of a reverse state machine which can use the date (month and day) as input and output the day of the year.

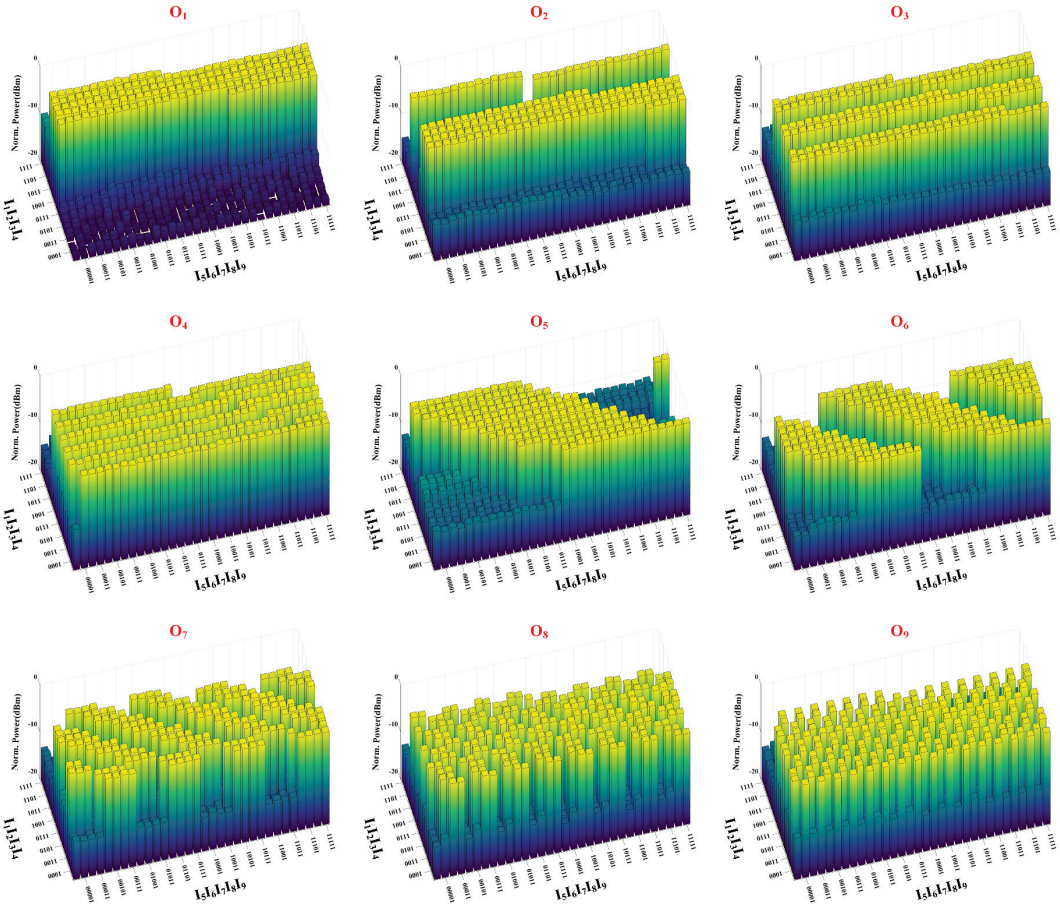

Fig. S5. The power distributions of the state machine to infer the date (month and day) according to the provided day of the year based on nine-input PLA, whose input is the day of the year ($I_1 \ldots I_9$), outputs are the month ($O_1 \ldots O_4$) and the day of the month ($O_5 \ldots O_9$)

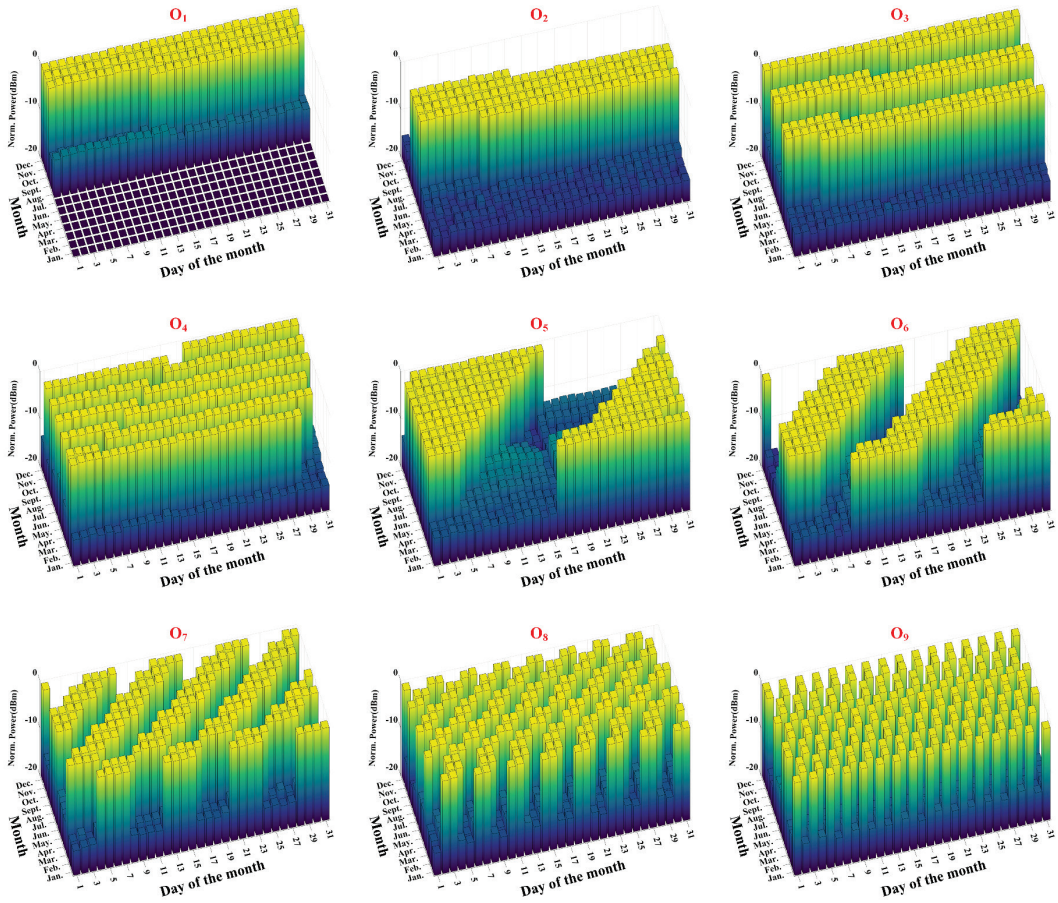

Fig. S6. The power distributions of the state machine to infer the day of the year according to the provided date (month and day) based on nine-input PLA, whose inputs are the month (I_1…I_4) and the day of the month (I_5…I_9), output is the day of the year (O_1…O_9).

S4: The measured truth tables for two-dimensional cellular automaton

Fig. S7 shows the power distribution (measured truth table) for Conway's Game of Life, based on nine-input PLA. It can be divided into two parts according to the operand I_5 (the state of the center cell). If the center cell is dead in the current iteration (I_5=0), the center cell can be live in the next iteration only if the three surrounding cells are alive (three of the other eight operands are 1). If the center cell is live in the current iteration (I_5=1), it can maintain live if two or three surrounding cells are live (two or three of the other eight operands are 1). The extinction ratio between the live and dead states of the cell is over 8 dB, which ensures the accuracy of the cell evolution in the experiment.

Fig. S8 depicts the power distributions (measured truth tables) for other kinds of two-dimensional CA implemented by PLA, the replicator-like evolution and the non-isotropic evolution. Since the center cell's current state will not affect its next state, we here give the truth table except for I_5 (the operand used to express the center cell's state) in Fig. S9(a). In the non-isotropic evolution, the top-left cell and the top-right cell will affect the next state of the center cell, which corresponds to the input operands I_1 and I_3 (highlighted in red). And the center cell's next state is live as long as the center cell's current state is live. Hence, the output results will be Logic 1 when the input operand I_5 is Logic 1.

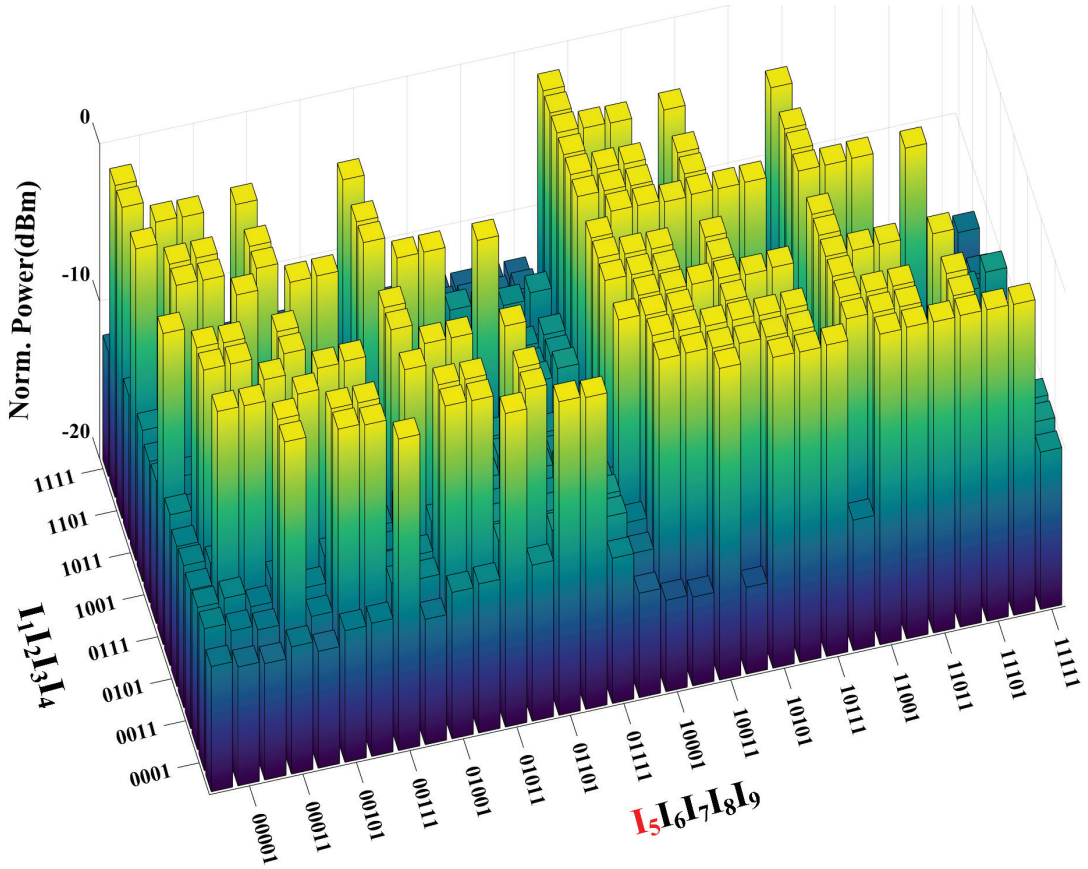

Fig. S7. Power distribution (measured truth table) for the Conway's Game of Life. Operand I_5 corresponds to the state of the center cell, and other operands correspond to the states of the surrounding cells.

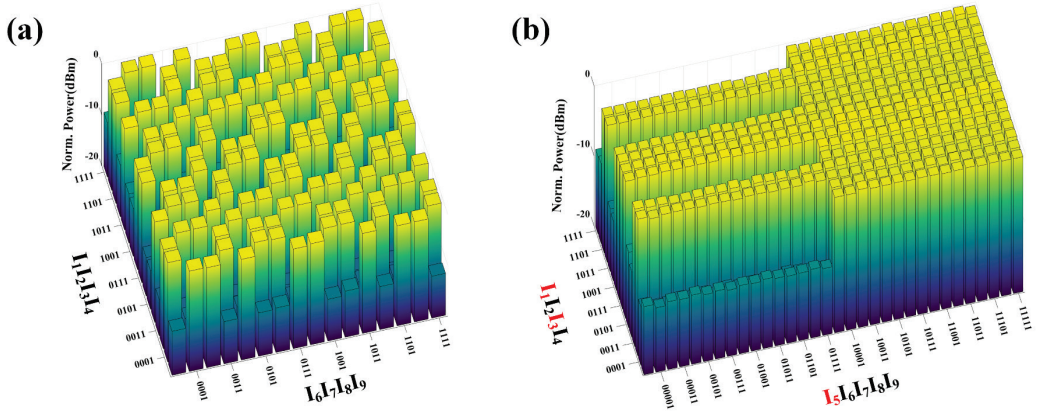

Fig. S8. Power distributions (measured truth tables) for other kinds of two-dimensional CA implemented by PLA. (a) The truth table for the replicator-like evolution. (b) The truth table for the non-isotropic evolution.

S5: Estimation of PLA's power consumption

In this section, we estimate the power consumption of PLA. One optical switch will consume about 0.1 pJ/bit based on thin-film lithium niobate[53]. For 8-input PLA at the speed of 10 Gbit/s, the dynamic power consumption is P_d=0.1 pj/bit×10 Gbit/s×8=8 mW. In the spectral modulator, the WSS can be replaced by the fixed filter with a square transmission spectrum of the corresponding period, whose loss can be optimized to about 1.5 dB[54]. The insertion loss of one optical switch is about 2.5 dB[55]. As a result, the total loss is 4 dB for one SM and 32dB for eight SMs. Since the minimal detectable power is 1 μW[56],

a single wavelength channel requires the laser power of about 1.6 mW. For 256 wavelength channels, the required laser power is 256×1.6 mW=409.6 mW. Therefore, the total power consumption is 417.6 mW. Considering 8-input PLA can simultaneously generate 256 minterms, the average power consumption of one minterm is 1.63 mW. Under the operation speed of 10 Gbit/s, the power consumption per bit is 0.163 pJ/bit.

S6: PLA's expansion principle of the combination between wavelength's and spatial dimensions

In this section, we present a feasible way to extend the size of the PLA by combining the wavelength's and spatial dimensions. Fig. S9(a) shows the schematic diagram of a four-input PLA. In the wavelength dimension, we load the first two operands (A, B) into the two cascaded SMs and obtain four minterms (M(A, B)) represented by four wavelengths. The M(A, B) is then input into a 1×2 OS, whose upper channel outputs are CM(A, B) and lower channel outputs are $\overline{\text{C}}M$(A, B). The two output ports are followed by two OSs to load the operand D. As a result, the four ports will output 16 minterms of 4 input operands. Fig. S9(b) shows the correspondence between the generated minterms and the wavelength's and spatial dimensions. The 16 minterms correspond to the 16 possible combinations between four wavelengths and four spatial ports. We can control the four WSs after the four output ports to select the minterms to realize the targeted logic operations.

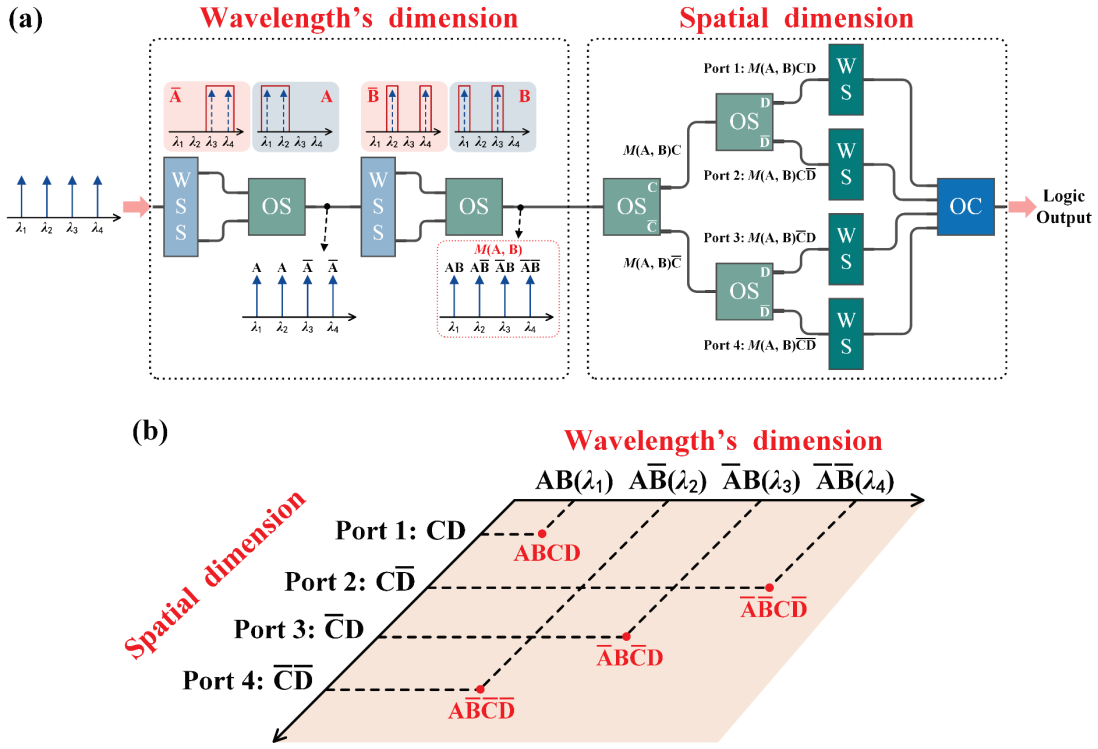

Fig. S9. Using the spatial dimension to increase the size of the PLA. (a) Schematic diagram of a four-input PLA by combining the wavelength and spatial dimensions. (b) The correspondence between the generated minterms and the two wavelength's and spatial dimensions.